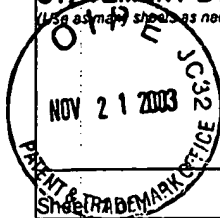


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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

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Complete if Known

Application Number	10/071373
Filing Date	February 8, 2002
First Named Inventor	Howard, Jason
Group Art Unit	2816 2124
Examiner Name	Unknown Chat

Attorney Docket No: 884.584US1

Technology Center 2100

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
AD	US-5,117,133	05/26/1992	Luebs, Richard	307	471	12/18/1990
CD	US-5,612,632	03/18/1997	Mahant-Shetti, S., et al.	326	46	11/29/1994
CD	US-5,867,049	02/02/1999	Mohd, Bassam	327	200	11/21/1996
CD	US-5,978,827	11/02/1999	Ichikawa, T	708	709	04/10/1996
CD	US-6,060,910	05/09/2000	Inui, S.	326	98	08/07/1998
CD	US-6,121,807	09/19/2000	Klass, E. F., et al.	327	210	05/24/1999
CD	US-6,181,180	01/30/2001	Chen, Zhanping, et al.	327	211	06/28/1999
CD	US-6,397,240	05/28/2002	Fernando, J S., et al.	708	603	02/18/1999
CD	US-6,437,602	08/20/2002	Friend, David, et al.	326	93	07/12/2001
CD	US-6,578,063	06/10/2003	Kojima, N, et al.	708	708	06/01/2000
CD	US-6,584,485	06/24/2003	Aoki, N, et al.	708	708	04/14/2000

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
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EXAMINER

DATE CONSIDERED

01/08/05

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Form 1449*	Atty. Docket No.: 884.584US1	Serial No. Unknown 10/071373
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Jason M. Howard et al.	
	Filing Date: Here with 02/08/02	Group: Unknown 8194

U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
CD	5,612,632	03/18/1997	Mahant-Shetti et al.	326	46	11/29/94
CD	5,764,089	06/09/1998	Partovi et al.	327	200	08/30/96
CD	5,898,330	04/27/1999	Klass	327	210	06/03/97
CD	5,900,759	05/04/1999	Tam	327	201	06/26/97
CD	6,242,952	06/05/2001	Bosshart et al.	326	98	09/24/99
CD	6,304,123	10/16/2001	Bosshart	327	212	08/02/00

FOREIGN PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes No
	01-206717	08/18/1989	Japan	H03K	3/37	X (abstract)

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

**Examiner Initial	Document
CD	Anonymous, "Power Saving Latch", <u>IBM Technical Disclosure Bulletin</u> , 39, 65-66, (Apr. 1, 1996)
CD	Beaumont-Smith, A., et al., "Reduced Latency IEEE Floating-Point Standard Adder Architectures", <u>Proceedings of the 14th IEEE Symposium on Computer Arithmetic</u> , 8 pgs., (1998)
CD	Elguibaly, F., "A Fast Parallel Multiplier-Accumulator Using the Modified Booth Algorithm", <u>IEEE Transactions on Circuits and Systems -- II : Analog and Digital Signal Processing</u> , 47 (9), pp. 902-908, (Sept. 2000)
CD	Even, G., et al., "On the Design of IEEE Compliant Floating Point Units", <u>IEEE Transactions on Computers</u> , Vol. 49, 398-413, (May 2000)
CD	Goto, G., et al., "A 54 X 54-b Regularly Structured Tree Multiplier", <u>IEEE Journal of Solid-State Circuits</u> , Vol. 27, 1229-1236, (Sept. 1992)
CD	Hokenek, E., et al., "Second-Generation RISC Floating Point with Multiply - Add Fused", <u>IEEE Journal of Solid-State Circuits</u> , 25 (5), pp. 1207-1213, (1990)
CD	Ide, N., et al., "2.44-GFLOPS 300-MHz Floating-Point Vector-Processing Unit for High-Performance 3-D Graphics Computing", <u>IEEE Journal of Solid-State Circuits</u> , Vol. 35, 1025-1033, (July 2000)
CD	Klass, F., "Semi-Dynamic and Dynamic Flip-Flops with Embedded Logic", <u>Proceedings of the Symposium on VLSI Circuits, Digest of Technical Papers</u> , Honolulu, HI, IEEE Circuits Soc. Japan Soc. Appl. Phys. Inst. Electron., Inf. & Commun. Eng. Japan, pp. 108-9, (1998)

Examiner 	Date Considered 01/08/05
--	--------------------------

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER. Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form 1449*

Atty. Docket No.: 884.584US1

Serial No. ~~Unknown~~ 10/07/373INFORMATION DISCLOSURE STATEMENT
BY APPLICANT

(Use several sheets if necessary)

Applicant: Jason M. Howard et al.

Filing Date: ~~Herewith~~ 02/08/02Group: ~~Unknown~~ 2124

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

**Examiner
Initial

CP Lee, K.T., et al., "1 GHz Leading Zero Anticipator Using Independent Sign-Bit Determination Logic", 2000 Symposium on VLSI Circuits Digest of Technical Papers, 194-195, (2000)

CP Luo, Z., et al., "Accelerating Pipelined Integer and Floating-Point Accumulations in Configurable Hardware with Delayed Addition Techniques", IEEE Transactions on Computers, 49 (3), 208-218, (March 2000)

CP Panneerselvam, G., et al., "Multiply-Add Fused Risc Architectures for DSP Applications", IEEE Pac Rim, pp. 108-111, (1993)

CP Partovi, H., et al., "Flow-Through Latch and Edge-Triggered Flip-Flop Hybrid Elements", Proceedings of the IEEE International Solid-State Circuits Conference, Digest of Technical Papers and Slide Supplement, NexGen Inc., Milpitas, CA, 40 pgs., (1996)

Examiner

Date Considered

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPBP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.